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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,144	03/30/2004	Tony M. Tarango	42P18570	5431

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,144	TARANGO ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed 03/30/2004. Claims 1-19 are pending and presently under examination.

Specification

The abstract of the disclosure is objected to because the last line, the expression "other embodiments are also described and claimed" should be deleted. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Mak et al. (US 6,885,209). The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e)

might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding independent Claim 1, Mak discloses a method for testing a data recovery circuit in a receiver 180, Figure 7 comprising:

Disturbing the phase of the data stream in the phase locked loop 1800, using a phase adjuster 182 to adjust the detected phase in a phase detector 1806, as the phase locked loop receives the incoming data stream with embedded clock (I and I#) at the differential sense amplifier 187, which converts the data stream to a single-ended wide-swing signal to be sent to the phase locked loop 1800.

Evaluating the width of the data eye of the transmitted data stream I and I# received from the transmitter 140, by adjusting the phase of the phase detector 1806 and moving the phase of the recovered clock from the phase locked loop 1800. An adjustment of the phase detector 1806 shifts the relative phase difference between the recovered clock and the incoming data stream. In the testing mode, the phase adjuster 182 adjusts the phase detector 1806 by adding phase delay, through adding capacitance to the phase detector to keep the clock and the signal out of phase.

Regarding Claim 2, Mak discloses using a phase adjuster 182 to adjust the detected phase in the phase detector 1806 to a value that represents a running phase the phase detector.

Regarding Claims 3, 4, Mak discloses receiver test register 160 for programming the phase value and threshold value at each strobe as the phase value and the threshold value are adjusted and examined by the receiver test register 160. To determine the size of the data eye, the phase and threshold values as programmed by the receiver test register 160 to reflect the adjustments by the phase adjuster 182 and the threshold shifter 184 are combined.

Regarding Claim 5, Mak discloses a pass/fail comparator 190, which compares the loop-back received signal from the receiver 180 against the data stream to the transmitter 140 for any mismatch as shown in Figure 5.

Regarding Claims 6, 7, Mak discloses an integrated circuit design validation and high volume manufacturing screening process, using simple digital controls and on-chip components to find the size of a data eye with a transmitted signal, and to stress test the receiver by stressing the transmitted signal, see Summary of the Invention.

Regarding independent Claim 8, Mak discloses testing the receiver 180 by programming the transmitter test register 120 to introduce noise and jitter into the signal transmitted by the transmitter 140 to the receiver 180 to determine the ability of the receiver 180 to synchronize jittering and degraded signals, as shown in Figure 8. The transmitter test register 120 is programmed such that the noise generator 142 introduces noise by varying the phase of the transmitted signal in the time domain, while the level shifter 144 shifts the voltage level of the transmitted signal to adjust the transmitted data in the voltage level domain.

The noise generator 142 introduces jitter into the transmitter 140 by jittering the system clock to introduce a jittered bit rate clock into the data stream input to the transmitter 140. The jittered bit rate clock is then input to the parallel to serial encoder 141 to obtain the jittered serial data, and then input to the differential driver 143, where the jittered differential data is output as the outgoing data stream I and I#, in order to determine the robustness of the receiver using the noise simulation as described above, Figure 9.

Regarding Claim 9, Mak discloses a pass/fail comparator 190, which compares the loop-back received signal from the receiver 180 against the data stream to the transmitter 140 for any mismatch as shown in Figure 5.

Regarding Claim 10, Mak discloses testing the receiver 180 by programming the transmitter test register 120 to introduce noise and jitter into the signal transmitted by the transmitter 140 to the receiver 180 to determine the ability of the receiver 180 to synchronize jittering and degraded signals, as shown in Figure 8. The transmitter test register 120 is programmed such that the noise generator 142 introduces noise by varying the phase of the transmitted signal in the time domain, while the level shifter 144 shifts the voltage level of the transmitted signal to adjust the transmitted data in the voltage level domain.

Regarding independent Claim 11, Mak discloses a method for testing a receiver 180, as shown in Figure 8, of an exemplary embodiment of the on-chip system 100 of Figure 4 in a receiver testing mode, where the receiver 180 is the device under test (DUT), and the transmitter 140 is the tester, the method comprising:

Programming the transmitter test register 120 to introduce noise and jitter into the signal transmitted by the transmitter 140 to the receiver 180 to determine the ability of the receiver 180 to synchronize jittering and degraded signals. A noise generator 142 and a level shifter 144 are provided in these exemplary embodiments, and the transmitter test register 120 is programmed such that the noise generator 142 introduces noise by varying the phase of the transmitted signal in the time domain, while the level shifter 144 shifts the voltage level of the transmitted signal to adjust the transmitted data in the voltage level domain.

Evaluating a data stream for an error, the data stream having been recovered by the receiver while the loop was affected by said jitter, using, as shown in Figure 5, a pass/fail comparator 190, which compares the loop-back received signal from the receiver 180 against the data stream to the transmitter 140 for any mismatch.

Regarding Claims 12-16, Mak discloses loading pre-determined values into the receiver and transmitter test registers 120 and 160, from the pattern generator, where if the receiver 180 produces data which mismatches the transmitted data from the pattern generator 110, as indicated by the pass/fail comparator 190, then the transmitter 140 may have faults that should be rejected.

As show in Figure 7, during the test mode incoming data stream I and I# with an embedded clock are provided to the phase locked loop 1800, and the recovered clock from the phase locked loop 1800 is input to the sense amplifier 181, which outputs recovered data to the buffer 183 and then decoder 185. An adjustment of the phase detector 1806 shifts the relative phase difference between the recovered clock and the

incoming data stream. In the testing mode, the phase adjuster 182 adjusts the phase detector 1806 by adding phase delay, through adding capacitance to the phase detector, or the like, to keep the clock and the signal out of phase. Thus, in the on-chip system 100 of Figure 5, the size of the data eye can be determined by the extent of the possible shift the relative phase of the recovered clock shifts with the data eye.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being obvious over Mak et al. (US 6,885,209) in view of Watanabe et al. al. (US 6,522,122).

Regarding independent Claim 17, Mak discloses an integrated circuit, including a transmitter 140 and a receiver 180, where the receiver 180 is the device under test (DUT), and the transmitter 140 is the tester, the integrated circuit, Figures 4, 5, 7 and 8, comprising:

A chip I/O interface to a serial point to point data link, such as a high speed serial link between the transmitter 140 and receiver 180 for transmitting and receiving high speed serial data, the interface having a receiver 180, which includes a differential

sense amplifier 187, which receives the incoming data stream with embedded clock I and I#, and converts the data stream to a single-ended wide-swing signal to be sent to the phase locked loop 1800. An advance/retard generator, such as a phase detector 1806 shifts the relative phase difference between the recovered clock and the incoming data stream. An offset control unit, such as a phase adjuster 182 to adjust the detected phase in the phase detector of a phase locked loop. The phase and threshold values as programmed by the receiver test register 160 to reflect the adjustments by the phase adjuster 182 and the threshold shifter 184 are combined. By combining the two adjustments, the size of the transmitted data eye in both the time domain and the voltage level domain can be determined, Figure 7.

Regarding Claims 17-19, Mak does not explicitly disclose "a digital to analog converter (DAC) control unit with an input coupled to an output of the advance/retard generator". However, it is well known in the art to use a DAC converter in the design implementation of the integrated circuits for the purpose of converting analog signals to signals. Furthermore, in analogous art, Watanabe discloses a jitter measuring device for measuring the on-time-base fluctuations of a pulse train in digital transmission or a clock signal from a semiconductor integrated circuit, including an A/D converter (24, Figure 2), which converts the output samples from the sampling circuit 14 to digital data corresponding to its level for each sampling clock.

Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a well-known DAC converter as taught by Watanabe in the testing apparatus of Mak, for the purpose of converting analog to

digital signals from a sampling circuit, since digital signals are flexible in the implementation of test systems.

Regarding Claims 18, 19, a mixer unit part of (VCO) 1802 and a digital filter (loop filter, 1808, Figure 7) coupled between a voltage-controlled oscillator (VCO) 1802, and a phase detector 1806.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 4/3/06

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